MANUFACTURING ROBUSTNESS OF CSP ON AN SMT LINE

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1. ABSTRACT

The JPL-led CSP Consortium of enterprises representing government agencies and private companies has jointed together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. Since last year, more than 150 test vehicles, single- and double-sided, have been assembled and are presently being subjected to various environmental tests. As an active participant in the consortium, Celestica has been heavily involved in test vehicles design review and test vehicle assembly. Its Customer Oriented Rapid Engineering Lab (CORE Lab) was used for assembly and inspection of the CSP test vehicles. Key objective was to integrate CSPs into main stream surface mount technology (SMT) assembly.

In this paper, the assembly process flow, solder paste for different stencil design, manufacturing defects, X-ray inspection results, and ultrasonic characterizations are reported. Optimize process techniques which were learned during the six month assembly of test vehicles are also presented. Also, manufacturing robustness of CSPs were investigated by increasing the placement offset during assembly. Limiting offsets for different CSPs were reported and finally, future activities on assembly process optimization and characterizations were reviewed.

Keywords: electronic assembly, SMT, CSP, fine pitch, microvia technology, BGA

2. INTRODUCTION

In recent years, chip scale packages (CSPs) have emerged as the packaging technology of choice, filling industry's continuous needs for smaller, faster and lighter performance electronics products. This technology has found many applications in the memory, telecommunications and aerospace industries. As an increasing number of manufacturers adopt it as an advanced package and more applications are found for it, the importance of understanding the issues associated with large scale assembly increases.

To investigate the many issues of implementing CSP technology and verifying its reliability, a consortium led by the Jet Propulsion Laboratory (JPL) was formed to design and build a test vehicle with different types and styles of CSP. Also, one of the Consortium's main goals was to find a way to integrate CSPs into mainstream SMT assembly. The large difference in size and pitch created many different challenges that needed to be addressed. This exercise provided valuable information regarding the inherent robustness and reliability of the CSPs.

As an in-kind contribution, Celestica was involved in the process development and test vehicle assembly. The test vehicle (TV) included eleven different CSPs in the assembly. Initially, manufacturing processes were more precisely defined by assemblying a number of trial test vehicles; at the beginning of full production, they were further optimized. The processes were further fine tuned during a six-month test vehicle build. The optimum screening parameters, placement program, and reflow profile were determined in order to minimize manufacturing defects. Post-assembly inspection played a very important part as a quality control tool as different optimization techniques were performed. A set of test vehicles was built to investigate CSP's manufacturing robustness by increasing the placement offsets from that of normal assemblies.

3. OBJECTIVES

In order for CSPs to become widely accepted in today's market, the assembly process has to be flexible enough to accommodate a variety of components: quad flat packages (QFPs), ball grid arrays (BGAs) and CSPs. Low I/O memory CSPs are widely accepted and are found to be easy to assemble due to the general lack of variety in components[1]. However, for medium I/O and application specific integrated circuit (ASIC) packages, it is much more challenging to accommodate CSPs into mixed technology assembly. Using its extensive experience in electronics assembly, Celestica's process development team aimed to develop a robust process compatible with the standard SMT assembly process while also minimizing manufacturing defects. The reliability of such processes also needed to be determined. In order for the process to be effective on a large scale, it became important to ascertain the allowable margin of errors that could still produce a reliable product.

4. EXPERIMENT

Over the six-month span of the project, minor modifications were made to the process. However, the primary SMT assembly process flow remained unchanged. This process flow is shown in Figure 1.

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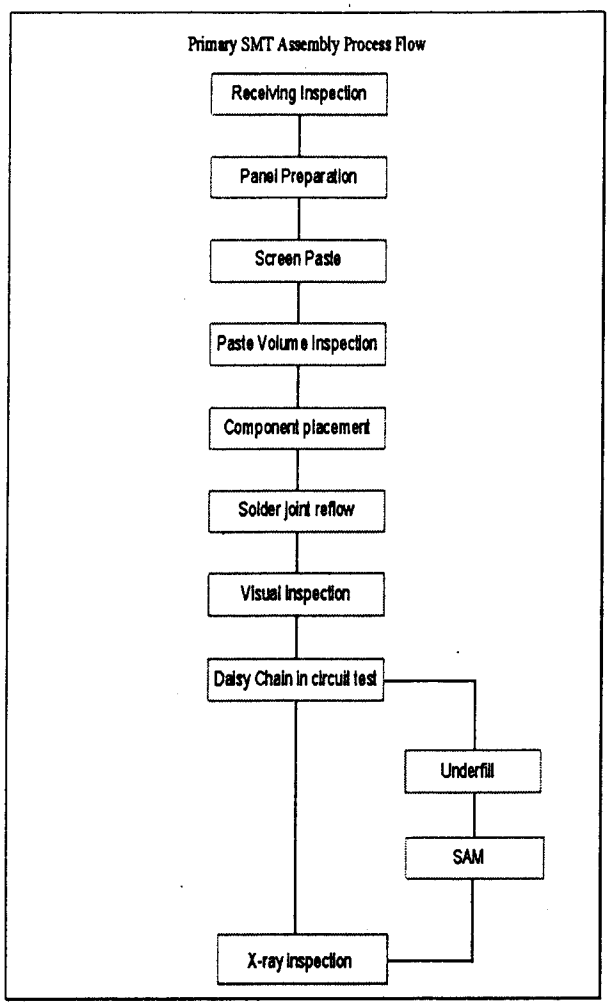


Figure 1. Primary SMT Assembly Flow

From a manufacturing point of view, the eleven CSPs used on the test vehicle were classified based on their basic structure. There were three basic types of CSP structures: leadless packages similar to leadless chip carriers (LCCs), leaded packages similar to a gull wing package, and grid packages similar to BGAs[2]. Table 1 lists the CSPs with their characteristics.

The printed wire boards (PWBs) were designed with microvia one side, and conventional design on the other. All soldering pads on the test boards were non-solder mask defined (NSMD). The use of such a board allowed the team to investigate the effects of microvia build up technology on assembly void levels in comparison to conventional technology under the same assembly conditions. Each assembly step will be discussed briefly as follows.

Receiving Inspection: CSPs and PWBs

All CSPs were inspected and screened for:

a) Physical package damage

Some of the CSPs exhibited damage due to handling and shipping. Delamination of the redistribution layer from the die was seen in some CSPs. Scratches were found on both sides of many of the CSPs.

b) Missing or deformed solder balls

Since most of the CSPs used were prototype, they were not packaged in tape and reel. Balls were damaged due to unsuitable carriers; they were pinched or flattened. All CSPs were visually inspected for missing balls. If missing balls are not detected, they can present a potential problem for the automated placement machines. Even though is not desirable, the automated vision system was programmed to detect missing balls. This is not acceptable for production assembly since it prolongs placement time, thus increasing assembly costs.

Table 1. CSPs Assembled

Package ID	Package Type	Package Type	Pitch mm
B	Leadless-1	Bottom Lead	0.8
C	TAB CSP-2	Full Array	0.75
D	TSOP44	Lead	0.8
E	Leadless -2	Bottom Lead	0.5
F	TAB CSP-1	Full Array	0.75
G	Chip-on-Flex-1 (COF-1)	Full Array	.020 in.
J	Wire bond on Flex-1	Peripheral	0.8
K	Wire bond on Flex-2	Peripheral	0.5
M	Chip-on-Flex-2 (COF-2)	Peripheral	.020 in.
N	Ceramic CSP	Full Array	0.8
O	Wafer Level	Peripheral	.020 in.

* All measurements are in mm unless otherwise specified

c) Organic residues

The majority of the CSPs received seemed to exhibit some form of organic residue. The area surrounding the solder balls was white and flaky. These organic residues were probably left over from previous package manufacturing processes, and they may have an effect on package solderability. CSPs with thick residues were cleaned in isopropanol (IPA) bath.

d) Polarity marks

Not all CSPs were received with a polarity marking. For asymmetrical CSPs, this did not present a problem as the placement machine was able to reject misoriented components. However, leaded packages, TSOPs and symmetric balled CSPs need an appropriate mark for proper component loading. Correct package polarity was assured by marking and placement at right orientation.

All PWBs were inspected for:

a) Warpage

Board warpage was observed on some boards. This could cause misprinting of solder paste, as well as false alarms in the solder volume measurement system. The resilient force

in severely warped boards would generate vibrations, causing placed modules to shift. IPC standards, IPC-TM-650, method 2.4.22, were followed for this type of inspection.

b) Missing solder mask dam or misregistration
In trial experiments, PWBs showed solder mask misregistration. Mask registration was significantly improved for full PWB production. Misregistration causes decrease in solder volume due to either partial coverage of solder pads and/or solder thieving with no coverage of copper traces. Existence of solder mask dam between pads is also critical. The elimination of the dam has been linked to the occurrence of solder bridging in fine pitch assemblies. The inspection process was performed manually using a light microscope to screen for such defects.

c) Microvia misregistration
In the case of partially registered microvias, the soldering pads were not fully connected with the internal circuitry of the PWB. This type of defect can be detected by electrical test after assembly, but its sources may not be determined if PWBs were not inspected prior to assembly. Again, this defect was observed more often in trial PWBs and it was minimized for full production. All PWBs were visually inspected for such defect and those with microvias at the pad edges were rejected.

Panel Preparation
The PWBs received did not need any preparation, as they were shipped precut. Packages B, D, and E, as level 3 (moisture sensitive, allowed one week out of bag at 30°C/60% RH), were processed with a 125°C moisture bake-out for 24 hours prior to assembly. The remaining CSPs did not require a moisture bake-out. All CSPs were stored in a dry nitrogen chamber prior to assembly to avoid any time dependent moisture effects.

Solder Paste Printing
Stencil design proved to be the most challenging part of screen printing [3]. As it is rare to find a board that contains CSPs exclusively, it was critical to take into account other SMT packages into the paste volume calculations. In general, a 6 mil to 8 mil stencil is required to deposit adequate amounts of solder paste for surface mount devices (SMDs). When CSPs become incorporated into standard assembly processes, soldering problems may arise. The finer pitch and pad size involved could cause solder bridging should the same stencil be used. In addition, the low print area aspect ratio causes a reduced solder paste release rate[4].

The use of appropriate stencil design can improve solder printing quality for CSPs and SMDs and meet their solder paste volume requirements. A step-down stencil was evaluated in early experiments. Although it allowed for the solder volume variations needed in mixed technology assembly, inconsistency in the solder volume deposited and higher solder volume variation were observed. Another solution was attempted, which consisted of optimizing the combination of stencil thickness and aperture size.

Based on previous experiments, a 6 mil stencil was chosen for 141 of the 150 test vehicle built. The print area aspect ratios ranged from 0.47 to 1.09. The aperture size to pad size ratio was optimized to maximize the solder volume without sacrificing process robustness. In order to ensure that adequate amounts of paste were deposited, the aperture shape became an important parameter. From prior builds, it was determined that a square aperture with rounded corners provided superior paste release characteristics in comparison to round apertures.

The clearance between the bottom of the CSPs and the surface of the board was found to vary from component to component. The minimum height was found to be as small as 1.2 mil [2]. Conventional inline deionized (DI) water cleaners can not adequately clean underneath such a component; therefore a no-clean paste was chosen. The no-clean paste had a 63/37 Sn/Pb particle size of -325+500 (Type 3) and a room temperature viscosity of 900 to 1000 kcps.

Although paste volume was an important parameter, it was impossible to accurately measure it using the automated inline machine. The conventional dog bone design found in BGA design no longer existed. The microvias eliminated the need for the usual via features that are used for reference in paste volume measurements. Solder paste heights rather solder paste volumes were measured manually using LSM machine.

Component Placement – Offset Experiment
To place fine pitch CSPs accurately without sacrificing placement accuracy, it is necessary to understand how much component placement offset can be tolerated. The objective of the offset experiment was twofold: (1) to determine repeatability and reliability of the placement machine, and (2) to establish the largest amount of placement offset that can be self-corrected by the molten solder surface tension during reflow.

Prior to the offset placement build, the placement machine was verified for placement accuracy and repeatability using two CSPs, Packages C and N (see Table 1). These CSPs proved to be the most reliable in the previous experiments because they were the only packages having uniform ball arrays. CSPs were placed on double sided tape twice and the offsets were measured manually using a microscope image. Initially, a "100% on pad" placement was repeated until a reliable result was achieved. An example of 50% offset that was achieved through repeatability can be seen in Figure 2.

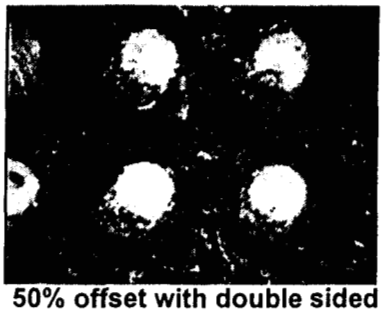


Figure 2. 50% offset with double sided tape

The placement machine was then programmed to place the packages at three different locations which were mathematically determined. These values were programmed such that it allowed for the package placement of 60, 65 and 70 percentages off pad. All offset percentages were once again verified using the double-sided tape method. Three boards at each offset percentage had solder paste deposited on them using a high precision printer, packages were placed and the boards were then reflowed. The printer gave excellent and repeatable paste placement with no requirement for additional adjustment.

Once reflow was completed, each assembly was extensively x-rayed to determine if the CSP had pulled back to the pad during the reflow process. X-ray inspection revealed that all CSPs aligned themselves on pads for 60, 65 and 70 percentage offsets. It was also found that placement accuracy and repeatability were dependent on three major factors: (1) the cleanliness and shininess of the CSP balls, (2) the pattern recognition method of the placement machine, and (3) the way the CSP fitted in its waffle pack carrier.

It is extremely important to ensure that the CSP solder balls are free from flux residue before placing them. CSPs can be cleaned in an IPA bath in order to clean the solder balls thoroughly. This ensures optimum contact between the solder ball and the pad, and thus reduces the placement machine vision system error.

Furthermore, pattern recognition also plays an important part in placement accuracy and reliability. There are two types of placement methods; each gives a different accuracy level: (1) four corner and row and (2) column recognition. It is much more desirable to use the latter since it provides a greater accuracy in picking and placement of the parts on the board, i.e., better machine vision recognition.

Another factor, seemingly minor, yet which causes many problems when the machine picks and places CSPs, is the CSP waffle pack carrier. It is very critical that the waffle pack walls adhere closely to the CSP dimensions so that package shifting and skewing do not occur within the waffle pack carrier as is being lifted.

For future experimental advances in this area, it is suggested that 100 cards or more should be utilized in order to have a statistically sound understanding of the effect of component offset due to the large amount of error which is incorporated into the experiment due to the small pad dimensions. It is also suggested that these components be placed at an increments of 2 to 5 percent added to 70 percent in order to determine the exact offset percentage where the molten solder can no longer pull the component back to the pad.

Solder Paste Reflow

For this project, a 10 zone convection reflow oven was used, having a nitrogen atmosphere controlled to less than 500 PPM oxygen level. No fixture or additional support was used as the test vehicle rode along the handling fingers of the oven. Any warpage incurred during reflow was then observed and measured.

Different thermal profiles were attempted during this project. It has been shown that a low thermal profile will reduce the percentage of solder voids[5]. The reflow profiles used were all within the boundaries of paste specifications provided by the supplier. Figure 3 shows the thermal profile in both sides of the control part on the assembly.

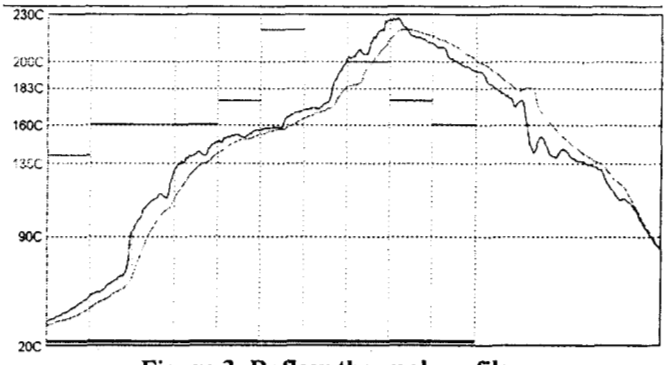


Figure 3. Reflow thermal profile

Underfill

Most CSPs on this test vehicle were not underfilled. The wafer level package (Package O, see Table 1) was the only CSP known to require underfilling. Thermal cycling test results shown in another paper in this Proceedings indicate a potential needs for underfill of a few other CSPs[6]. Three different types of underfill were used. Two types of commercially available underfill materials and one proprietary underfill material were used. The performance of each of these underfill materials was carefully observed. A pneumatic manual dispenser with syringe was used with a needle gauge of 22. The dispense pattern consisted of an I-shape. The underfill material was cured for 3.5 hours at 120°C.

Post-assembly Inspection

Both destructive and non-destructive techniques were used to inspect the assembled boards. Visual inspection was used in order to detect any damage sustained by the board and/or CSPs due to the assembly process. Standard light microscopy was used in conjunction with cross sectioning to examine solder joint quality. The test pads on the test vehicle were also probed for electrical discontinuities

(daisy- chain test). X-ray inspection was performed to detect manufacturing defects: solder bridging, solder balls, insufficient solder, solder wicking, and misregistration on the board surface. The scanning accoustic microscope (SAM) from Celestica's Materials Lab was used to inspect the underfill for voids, as well as part delamination.

5. DISCUSSION

Some of the defects could have occurred due to problems inherent in either the CSPs or the boards that could not be detected by visual inspection.

Receiving Inspection

Of the parts that were received, some were found to be damaged. It is apparent that a better way to package CSPs is necessary in order to reduce the number of damaged components. This would reduce the cost, as well as improve turnaround time because rigorous incoming inspection would no longer be needed.

Solder Paste Printing

Due to progress made from previous builds, the optimum 6 mil stencil was designed and used during the experiment. It was found that the print quality and consistency also depended on the quality of the solder paste and screen printer used. Originally, a commonly used no-clean paste was applied. Although satisfactory, the print quality was greatly improved upon changing the paste to a newer type of no-clean paste. Switching from a conventional printer to a later model printer also improved the consistency and quality of the screening process. The later model printer is equipped with a pressurized solder paste dispensing head. And it has an alignment repeatability of 6σ at 25 μm, and a print accuracy of 3σ at 25 μm. Figure 4 shows the paste screened onto a component site.

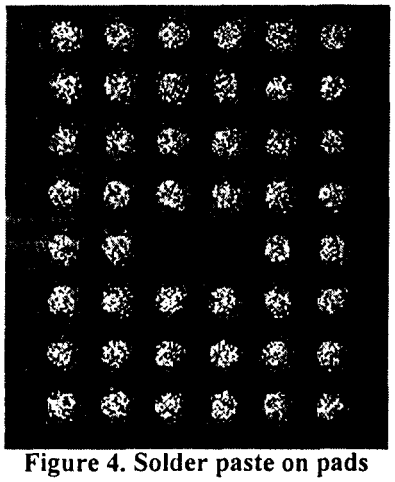


Figure 4. Solder paste on pads

Solder Paste Reflow

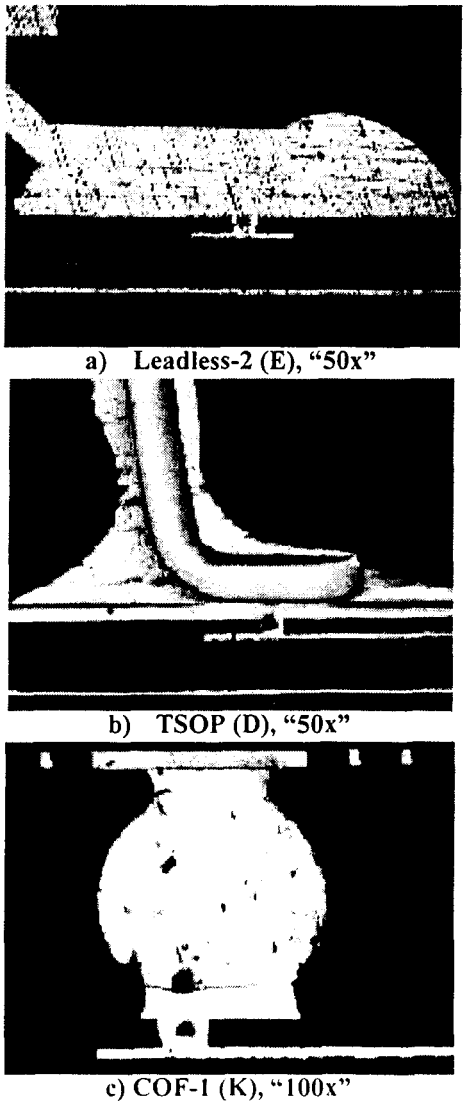
With the use of different thermal reflow profiles, the number of voids present in the joints changed. Solder joint integrity could be undermined by the location and size of those voids. Excessive voiding reduces the amount of solder at the joint and can affect reliability. However, entirely eliminating voiding is not necessary since if they are in the benign location, they could increase the package standoff, thus improving solder joint reliability.

Post-assembly Inspection

a) Cross-sectioning

Cross sectioning was performed on a board that passed the daisy-chain electrical continuity test. Solder voiding was observed, as expected from flux outgassing during reflow. Some of these voids were directly associated with the microvias. Most of the voids were found not to exceed one quarter of the solder joint's diameter. Figure 5 shows the joints for each of the package styles.

Note the voids in Figure 5c. The standoff height was also determined by examining the cross-section under a high magnification light microscope.



a) Leadless-2 (E), "50x"

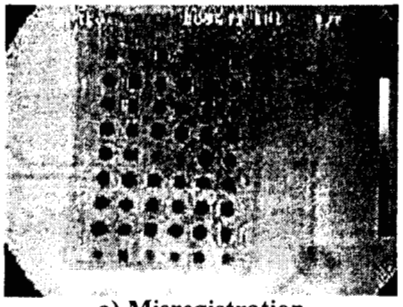
b) TSOP (D), "50x"

c) COF-1 (K), "100x"

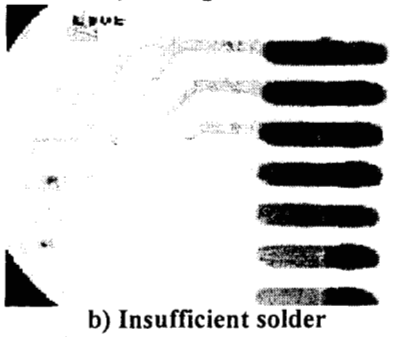
Figure 5. Cross section photomicrographs of assembled CSPs

c) X-ray inspection

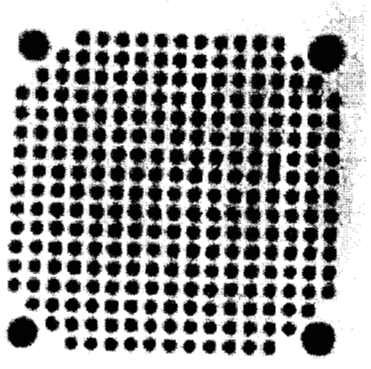
X-ray inspection was performed on assemblies that did not pass electrical probing. Major causes of failures that were detected include: CSP misregistration, solder bridging, and insufficient solder. Figures 6 show some of these fails.



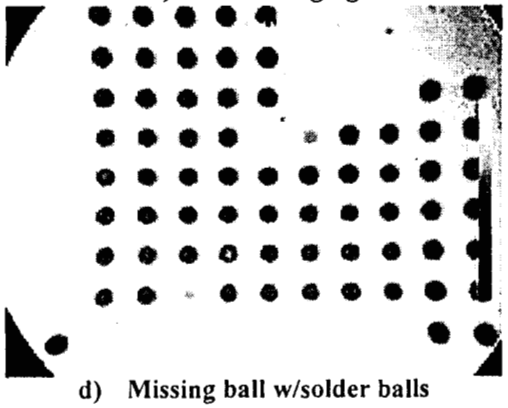
a) Misregistration



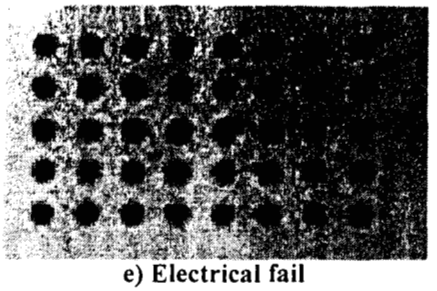
b) Insufficient solder



c) Solder bridging



d) Missing ball w/solder balls



e) Electrical fail

Figure 6. Defects observed using 2-D X-ray

All these defects were considered to be due to the assembly process. Voiding, though observable through x-ray, was not considered to be caused by a process deficiency as the amount of voiding can be controlled by altering the reflow profile with respect to the solder paste type. There were some occurrences of missing balls causing failure, though this was relatively rare. As stray solder balls were often found in the immediate vicinity, one possible explanation for the missing balls was that excessive outgassing through the microvia caused the solder ball to explode.

Figure 6d shows a CSP with a missing solder ball. As effective as X-ray was found to be, it also has its limitations. Figure 6e shows a CSP which failed electrical probing, yet no defect can be found. It is possible that the defect exists in the z-direction, and therefore cannot be detected with 2-D x-ray. However, the possibility of a faulty CSP cannot be ruled out.

e) Scanning acoustic microscope (SAM) inspection

SAM is a system that was designed primarily for the inspection of microelectronic devices. The system uses a pulse echo and through-transmission techniques of ultrasonic inspection; it operates over a frequency range of 5 to 150 MHz. Using SAM, it was found that some of the assemblies had voids and some had delamination. Delamination occurred on both surfaces of underfill material. Figure 7 is a SAM image taken of Package O (wafer level CSP) exhibiting delamination.

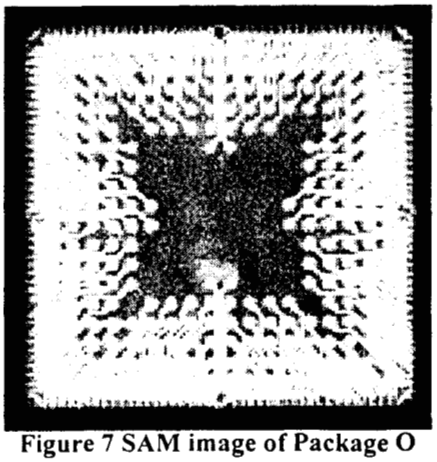


Figure 7 SAM image of Package O

6. CONCLUSIONS

- Tape-and-reel packaging for the CSPs should be used to improve the parts handling and placement effectiveness.
- It is possible to meet the solder volume requirements without using a step-down stencil. The use of a step-down stencil was found to introduce other operation-related variables to the soldering process. By optimizing the stencil thickness and aperture size, it was possible to deposit enough paste to accommodate CSPs as well as standard SMDs.
- The use of a high quality paste and printer can greatly improve print consistency and yield
- In order to measure the solder volume accurately using an automated system, reference pads need to be added when using microvia technology on PWBs.
- Low I/O grid CSPs have high process reflow tolerance, e.g., up to 70% pad offset placement was accommodated.
- A longer thermal profile will reduce, but not eliminate, voids in solder joints.
- Proprietary flip chip underfill material gives less voiding and delamination.

7. FUTURE WORK

As the CSP assembly development proceeds, reliability data emerges. According to reliability data and failure analysis, key assembly features will be finalized. With defined key assembly features such as standoff, solder joint dimension and grain, a matrix of assembly process parameters will be generated. For example, the solder volume is a function of the following: soldering pad size, solder paste type, and stencil aperture features.

Solder paste deposition
It has been shown that forty percent of the soldering defects were associated with the solder paste printing process in SMT assembly. Many techniques have been developed to inspect the printing quality. Therefore, there are methods to improve the solder paste deposition quality. The ultimate goal is to have a robust solder paste deposition process with position precision and volume consistency.

In the next test vehicle (TV2) design, a grid of calibration traces have been imbedded. Those traces will be used in the solder volume measurement experiment. A 3D laser measuring system will be employed. For each solder joint, there will be solder volume data to correlate directly to reliability data. In production, the solder paste inspection machine will be programmed to have a tight window with projected solder volume. Stencil materials and aperture cutting procedures affect the release rate of the solder paste. Chemically etched, laser cut and nickel-additive stencils will be evaluated in the design of experiment (DOE). Experiment will also include investigation of the aspect ratio of the stencil aperture with respect to the solder paste type and application method.

Thermal reflow profiling
Solder voiding and grain size may affect solder joint integrity. With varied thermal reflow profile according to solder paste type, solder voiding could be controlled. With available solder joint reliability data, controlled solder voiding will be expected.

3D solder joint inspection
3D solder joint inspection has been applied to most fine pitch SMT, CSP, and BGA assemblies. A subproject has been proposed to apply on grid CSPs. The most challenging aspect is to set the right threshold with the right calibration.

Underfill effectiveness
Underfill voids were observed occasionally for wafer level CSP assembly. The size and location of those voids could be varied by different underfill material dispensing procedures. In previous experiments, faster dispensing is always associated with a higher risk of introducing voids. In high volume production, optimizing the underfill process is a very important factor regarding throughput. After the underfill failure analysis is finished, a set of experiments will be conducted to optimize the underfill process.

8. ACKNOWLEDGEMENTS

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